Amendments to the Claims:

Please amend claims 1, 8 and 12 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A fuse circuit for a semiconductor integrated circuit, comprising:

a plurality of fuses; and

a like plurality of transmission circuits, each of the plurality of fuses being coupled to only one corresponding transmission circuit of the plurality of transmission circuits; each transmission circuit having a single input at an input node and a single output at an output node for transferring signals from [[an]]the input node to [[an]]the output node in response to a status of the corresponding fuse, the input and output nodes of respective transmission circuits being coupled such that the transmission circuits are arranged in series, such that an input signal applied to the input node of a first transmission circuit in the series is transferred to the output node of a last transmission circuit in the series when all of the transmission circuits in the series are in an active state and such that the input signal is not transferred from the input node of the first transmission circuit to the output node of the last transmission circuit in the series when at least one of the transmission circuits in the series is in an inactive state.

2. (previously presented) The fuse circuit of claim 1, wherein each fuse in the plurality of fuses has an identical fusing status.

3. (previously presented) The fuse circuit of claim 1, wherein each of the fuses includes first and second terminals, the first terminal of each being connected to a first power supply voltage.

4. (previously presented) The fuse circuit of claim 3, wherein each of the transmission circuits comprises:

a transmission gate having an input terminal coupled to a corresponding input node, an output terminal coupled to a corresponding output node, and a primary control terminal connected to the second terminal of the corresponding fuse, and a secondary control terminal; and

an inverter having an input terminal connected to the second terminal of the corresponding fuse and the primary control terminal, and having an output terminal connected to the secondary control terminal.

5. (previously presented) The fuse circuit of claim 4, wherein the transmission gate includes:

a first conductive transistor having a first electrode connected to the input terminal, a control electrode connected to the second terminal of the corresponding fuse, and a second electrode connected to the output terminal; and

a second conductive transistor having a second electrode connected to the input terminal, a control electrode connected to the output terminal of the inverter, and a first electrode connected to the output terminal.

6. (previously presented) The fuse circuit of claim 4, wherein the first power supply voltage is applied to the input terminal of the first in the series of the plurality of the transmission gates.

7. (previously presented) The fuse circuit of claim 5, wherein each of the transmission circuits further comprises a resistor having a first terminal that is connected to the control electrode of the first conductive transistor and to the input terminal of the inverter, and having a second terminal that is connected to a second power supply voltage.

8. (currently amended) A fuse circuit storing information related to a semiconductor integrated circuit, comprising;

a plurality of fuses each of which has first and second terminals, the first terminal of each being connected to a first power supply voltage, the fuses each storing predetermined information relevant to the semiconductor integrated circuit; and

a like plurality of transmission circuits, each transmission circuit having a single input at an input terminal and a single output at an output terminal, a second terminal of each of the plurality of fuses being connected to only one corresponding transmission circuit of the plurality of transmission circuits, each transmission circuit transferring an input signal received at [[an]]the input terminal to [[an]]the output terminal in response to the predetermined information established by a status of the corresponding fuse,

wherein the transmission circuits are connected in series, such that an input signal applied to the input terminal of a first transmission circuit in the series is transferred to the output terminal of a last transmission circuit in the series when all of the transmission circuits in the series are in an active state and such that the input signal is not transferred from the input terminal of the first transmission circuit to the output terminal of the last transmission circuit in the series when at least one of the transmission circuits in the series is in an inactive state.

9. (previously presented) The fuse circuit of claim 8, wherein the plurality of fuses in combination store one-bit of the predetermined information relevant to the semiconductor integrated circuit.

10. (previously presented) The fuse circuit of claim 8, wherein each of the transmission circuits comprises:

a transmission gate having an input terminal, an output terminal, a primary control terminal connected to the second terminal of a corresponding fuse, and a secondary control terminal; and

an inverter having an input terminal connected to the second terminal of the corresponding fuse and the primary control terminal, and an output terminal connected to the

secondary control terminal.

11. (previously presented) The fuse circuit of claim 10, wherein the transmission gate includes:

a NMOS transistor having a drain connected to the input terminal, a gate connected to the second terminal of the corresponding fuse, and a source connected to the output terminal; and

a PMOS transistor having a source connected to the input terminal, a gate connected to the output terminal of the inverter, and a drain connected to the output terminal.

12. (presently amended) The fuse circuit of claim 11, wherein each of the transmission circuits further comprises a resistor having a first terminal that is connected to the control electrode of the NMOS transistor and the input terminal of the inverter, and having a second terminal that is connected to [[the]]a second power supply voltage.